Assignee: Intel Corporation

IN THE CLAIMS

Presented below is a complete listing of the claims.

1   Claims 1 through 19   (cancelled)

1   20.   (Currently amended) An apparatus, comprising:

2   a first register file of a plurality of register files <u>to be assigned for</u>

3 <u>register renaming in an out-of-order processor</u> to store predicate values;

4 and

5   a second register file of said plurality of register files to receive

6 results from execution of a first instruction that writes to multiple

7 predicate registers when said first register file is busy.

1   21.   (Previously presented) The apparatus of claim 20, further

2 comprising a select register to indicate which of said plurality of register

3 files is being written to by execution of a second instruction that writes

4 to multiple predicate registers.

1   22.   (Previously presented) The apparatus of claim 21, wherein

2 said select register includes a pointer to said which of said plurality of

3 register files.

1   23.   (Previously presented) The apparatus of claim 20, wherein

2 said first register file indicates that is it busy with a scoreboard.

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1   24.   (Previously presented) The apparatus of claim 23, wherein

2   said apparatus stalls execution of a third instruction that writes to at

3   most two predicate registers when said scoreboard indicates destination

4   registers of said third instruction are busy.

1   25.   (Previously presented) The apparatus of claim 20, further

2   comprising a free file list to point to the next in order of said plurality of

3   register files that is not busy.

1   26.   (Previously presented) The apparatus of claim 25, wherein

2   said free file list indicates which of said plurality of register files are to

3   be de-allocated.

1   27.   (Currently amended) A method, comprising:

2   storing predicate values in a first register file of a plurality of

3   register files to be assigned for register renaming in an out-of-order

4   processor; and

5   allocating a second register file to receive results from execution

6   of a first instruction that writes to multiple predicate registers when

7   said first register file is busy.

1   28.   (Previously presented) The method of claim 27, further

2   comprising indicating which of said plurality of register files is being

3   written to by execution of a second instruction that writes to multiple

4   predicate registers.

1   29.   (Previously presented) The method of claim 28, wherein

2   said indicating includes using a select register to point to said which of

3   said plurality of register files.

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1   30.   (Previously presented) The method of claim 27, further
2   comprising indicating busy status with a scoreboard.

1   31.   (Previously presented) The method of claim 30, further
2   comprising stalling execution of a third instruction that writes to at
3   most two predicate registers when said scoreboard indicates destination
4   registers of said third instruction are busy.

1   32.   (Previously presented) The method of claim 27, further
2   comprising pointing to a next in order one of said plurality of register
3   files that is not busy.

1   33.   (Currently amended) The method of claim 32, further
2   comprising de-allocating one of said plurality of register files when said
3   pointing indicates a an earlier in order one of said plurality of register
4   files is not busy.

1   34.   (Currently amended) A system, comprising:
2   a processor including a first register file of a plurality of register
3   files to be assigned for register renaming in an out-of-order processor to
4   store predicate values, and a second register file of said plurality of
5   register files to receive results from execution of a first instruction that
6   writes to multiple predicate registers when said first register file is busy;
7   an interface logic to couple said processor to input/output
8   devices; and
9   a disk drive logic coupled to said processor via said interface
10 logic.

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1   35.   (Previously presented) The system of claim 34, wherein
2 said processor includes a select register to indicate which of said
3 plurality of register files is being written to by execution of a second
4 instruction that writes to multiple predicate registers.

1   36.   (Previously presented) The system of claim 34, wherein
2 said first register file indicates that is it busy with a scoreboard.

1   37.   (Previously presented) The system of claim 36, wherein
2 said processor stalls execution of a third instruction that writes to at
3 most two predicate registers when said scoreboard indicates destination
4 registers of said third instruction are busy.

1   38.   (Previously presented) The system of claim 34, wherein
2 said processor includes a free file list to point to the next in order of
3 said plurality of register files that is not busy.